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IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,594	LEE, VAN HOA	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-16,18-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9-11,14-16,18-20,23-25 and 27-30* is/are rejected.

7)☒ Claim(s) *8,17 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the appeal brief filed on 14 March 2007. Claims 1-7, 9-16, 18-25 and 27-30 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5, 10, 14, 19, 23, and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawkins et al. [US 2002/0124194 A1] (hereinafter "Dawkins").

Per claims 1, 10 and 19, Dawkins teaches a method in a data processing system for providing valid translation entries in a translation control entry table (TCE facility and TCE Table, see Pg. 4, Para. [0043], [0044], [0046]) for all supported direct memory addresses, comprising:

reserving a page in system memory ("a reserved page per image ... ", see Pg. 4, Para. [0046]) for form a reserved page (the reserved page clearly must be formed first before being pointed to);

writing the reserved page (a page of memory is written to when a write operation from the operating systems addresses a memory range within the page);

selecting a region in system memory for the translation control entry table (the TCE table must be stored somewhere in system memory for the Hypervisor and the operating systems to access it, see Pg. 4, Para. [0046]); and

initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page ("initializes all entries in ... TCE table to point to a reserved page ... ", see Pg. 4, Para. [0044] and [0046]).

It is also clear the data processing system of claim 10 is already substantially disclosed above, as well as the computer program product in a recordable-type medium ("software", see Pg. 5, Para. [0050] and [0051]; "computer instructions", see Pg. 6, Para.[0066], [0068], [0076] and Pg.7, Para.[0077]) of claim 19.

Per claims 5, 14 and 23, Dawkins further teaches the page in the system memory and the reserved page are inaccessible to an operating system running on the data processing system (the reserved page is owned by an OS image, not by "one of the other OS images", see Pg. 4, Para. [0046]).

Per claims 28-30, Dawkins further teaches the reserved page is utilized for DMA address translation (Page 4, Paragraphs [0041], [0046] and [0047]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins et al. [US 2002/0124194 A1] (hereinafter "Dawkins"), further in view of Im [US 6,675,329 B1] (hereinafter "Im").

Per claims 6, 15 and 24, Dawkins does not specifically teach writing the reserved page includes setting all bytes within the reserved page to 0xFF. Im teaches writing all bytes within a memory to 0xFF in order to test the memory's accuracy (see Im, col. 5, lines 56-67 and col. 6, lines 1-5). Therefore, it would have been obvious to one ordinarily skilled in the art to combine Dawkins' and Im's teaching in order to test the accuracy of Dawkins' memory.

6. Claims 7, 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins et al. [US 2002/0124194 A1] (hereinafter "Dawkins"), in further view of

Tanenbaum et al. [Operating Systems: Design and Implementation] (hereinafter "Tanenbaum").

Per claims 7, 16 and 25, Dawkins does not specifically teach setting all valid bits to "1". However, Tanenbaum teaches an address translation mechanism (TLB, see Tanenbaum, Pg. 328, Fig. 4-12) that sets valid bits of its table entries to "1" to indicate the entries are valid (in use, see Pg. 328, Ln. 20-21). Since Dawkins initializes its TCE table entries to contain the address of the reserved page as described in claim 1, the entries are in use and therefore valid. Hence, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to associate valid bits to the table entries and set the bits to "1" to indicate that the entries are valid (in use).

7. Claims 9, 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins.

Per claims 9, 18 and 27, Dawkins does not specifically teach the size of the TCE table, the number of table entries, or the size of the table entries. However, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that these specific values are dictated by design choices and system parameters such as the size of system memory, page size, addressing format and performance costs.

Allowable Subject Matter

8. Claims 2-4, 11-13 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 5-7, 9, 10, 14-16, 18, 19, 23-25 and 27-30 have been considered but are moot in view of the response to argument below and the new ground(s) of rejection for claims 6, 15 and 24.

Applicant's arguments, see pages 22-24 of the appeal brief, filed 14 March 2007, with respect to claims 2, 3, 11, 12, 20 and 21 have been fully considered and are persuasive. The rejection of claims 2, 3, 11, 12, 20 and 21 has been withdrawn.

This Office action is not made final as the Examiner introduced new grounds of rejection.

10. Appellant's first and second arguments regarding claims 1, 10 and 19, on pages 10-13 of the appeal brief, that Dawkins fails to disclose the feature of "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page" is clearly erroneous.

In the Advisory Action mailed on 6 February 2007, the Examiner pointed out that the associated section of the TCE table disclosed by Dawkins is considered to be a TCE table that anticipates the Appellant's TCE table. As a result, the Appellant's

arguments directed to the above feature are moot due to the cited disclosure on page 11 of the appeal brief (Dawkins, paragraph 46), where Dawkins teaches initializing "all entries in a particular I/O adapter's associated section of the TCE table to point to a reserved page per image that is owned by the OS image that is allocated to that I/O adapter". Since Dawkins' invention provides the means to distinguish the sections of the overall TCE table by the particular I/O adaptors the sections belong to, and a table as understood by one ordinarily skilled in the art must contain at least one row of one or more entries or one column of one or more entries, it is clear that the sections can all be reasonably considered as TCE sub-tables or TCE tables for their respective I/O adaptors. The Appellant argues that Dawkins does not disclose that a section of a TCE table is itself a TCE table (see appeal brief, page 15, last three lines). However, the broadest reasonable interpretation of a TCE table is a table that contains TCE data/entries. Therefore, Dawkins' full TCE table is a TCE table in its strictest sense, the sections associated with the I/O adapters are also TCE tables in view of the broadest meaning of the term.

The Appellant is also respectfuly reminded that TCE entry data that points to a particular reserved page is valid data in view of the broadest and reasonable meaning of the term "valid". Assigning/initializing an entry to point to a particular reserved page is a valid assignment with valid data values. The Appellant seems to limit valid initialization to only mean setting valid bits associated with the TCE table to "1", which is what dependent claims 7, 16 and 25 recite. However, the independent claims 1, 10 and 19 do not recite or even hint "valid bits" and "setting valid bits to 1" as what the

Appellant may be suggesting the claims encompass. Instead, claims 1, 10 and 19 only call for initializing all entries of a TCE table to some valid value, and the all of the entries contain the address of the reserved page. In addition, the Appellant raised the issue of whether any subsequent DMA translation may still result in an unrecoverable error because of an invalid entry in the TCE table (see page 13, paragraph 3, lines 8-10 of the appeal brief). This issue is irrelevant to the scope of the claim and should not affect the interpretation of the claimed invention by one of ordinarily skill in the art. Dawkins teaches explicitly that the entries are initialized to point to a particular reserved page, and the values (pointers/addresses) that point to a particular reserved page are valid values. The Appellant also misinterpreted the Examiner's argument in the previous Office action by stating that "the Examiner appears to assert that Dawkins teaches initializing all entryes in the TCE to be valid ... because Dawkins teaches initializing TCE entries to prevent errors" (see appeal brief, page 17, paragraph 2 to page 18, paragraph 2). The Examiner makes no such assertion and the Appellant's argument regarding this issue is irrelevant.

Therefore in view of the broadest reasonable interpretation of the claim by one of ordinary skill in the art, Dawkins teaches "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page".

Appellant's second argument regarding claims 1, 10 and 19, on pages 13-14 of the appeal brief, that Dawkins fails to disclose the feature of "selecting a region in the

system memory for the translation entry table" is clearly erroneous. The first issue requiring clarification is what constitutes "the system memory", and the Examiner considers all of the memory locations in the system of Dawkins' invention form the system memory. The second issue is what constitutes an act of "selecting a region in the system memory". Dawkins may not have explicitly taught how the storage location of the TCE table is chosen, but it is clear that the TCE table must be stored in the system memory. The matter of how the location is selected/chosen is irrelevant. The location could be randomly selected or selected based on a particular algorithm or criterion, but it is nevertheless "selected". A particular memory address must be pointed to by the mechanism that stores the TCE table in the system memory. Therefore in view of the broadest reasonable interpretation of the claim by one of ordinary skill in the art, Dawkins teaches "selection a region in system memory for the translation control entry table".

Appellant's third argument regarding claims 1, 10 and 19, on page 14 and page 19 (see the last two paragraphs) of the appeal brief, that Dawkins fails to disclose the feature of "writing the reserved page" is clearly erroneous.

In Dawkins, on page 4, paragraph 43, Dawkins discloses "the TCE facility is for the **I/O** ... the TCE facility provides a mechanism to translate a contiguous address space on the **I/O** bus to a different an possibly noncontiguous address space in memory ... breaks the address space of the memory and the address space of the **I/O** bus into small chunks, call **pages**." On page 4, paragraph 44, Dawkins further discloses "when

an **I/O** operation starts on the bus, the TCE facility accesses the entry for that **page** in the TCE table ..." and "determine which page in memory is addressed, and the address bits taken from the **I/O** bus determines that address within the **page**". Also in Dawkins, page 4, paragraph 46, Dawkins discloses initializing "all entries in a particular **I/O** adapter's associated section of the TCE table to point to a **reserved page** per image that is owned by the OS image that is allocated to that **I/O** adapter". The Appellant is respectfully reminded that the term "I/O" encompasses both reading and writing.

Therefore, the act of "writing the reserved page" is clearly taught by Dawkins. The I/O operations from the OS image that owns the reserved page access the reserved page and write operations from the OS image constitution the act of "writing the reserved page". When the OS image performs a read operation from the reserved page, the retrieved data will be placed on the I/O bus, which also constitutes "writing the reserved page". In other words, both "writing to" and "writing from" the reserved page are considered to be "writing the reserved page".

Appellant's argument regarding claims 7, 16 and 25, on pages 26-27 of the appeal brief that there is no motivation to combine the references is clearly erroneous. Dawkins teaches the "TCE facility is a facility for the I/O which is analogous to the virtual memory address translation facility provided by most processors today" (see Dawkins, page 4, paragraph 43, lines 1-3), and Tanenbaum teaches an address translation mechanism (the Translation Lookaside Buffer) that sets valid bits of its translation table entries to "1" to indicate the entries are valid. Therefore, the

Appellant's argument for lack of motivation and non-analogous art is moot. The inventions of Dawkins and Tanenbaum share a common aspect in providing address translation for memory page access, and motivation to combine the references is valid to one of ordinary skill in the art. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Appellant's argument regarding claims 9, 18 and 27, on pages 33-34 of the appeal brief that Dawkins "does not teach, suggest, or give any incentive to make the needed changes to reach claim 9" is clearly erroneous. Dawkins states "the TCE facility ... uses the data in that entry as the most significant bits of the address to access memory ... " and "with the least significant bits being taken from the I/O address on the bus" (see Dawkins, page 4, paragraph 44). Dawkins also teachings in paragraph 44 that the number of bits taken from the bus is dependent on the size of the page, the TCE provides bits to determine which page in memory is addresses and the address bits taken from the I/O bus determines the address within the page. Therefore it is clear to one of ordinary skill in the art that the particular number of bits used to address a byte

or a word in the memory system is dependent on the size and number of the unit of data and the size of the address space. The bit length of the TCE table entry is dependent on the number of pages in the system, and this number is dependent on the page size and the size of the memory address space. The number of entry in the TCE table is also dependent on the number of pages, page size, and address space size. Therefore, it is obvious to one of ordinarily skilled in the art that the number of TCE table entries and the bit length of the entries are completely design dependent and motivated by the designer's choices of page size and address space size.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

6 July 2007

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100